UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,715	09/12/2001	Ping-Sheng Tseng	VD/017C10	8847

54698 7590 01/26/2007		EXAMINER
RAYMOND R. MOSER JR., ESQ.		
MOSER IP LAW GROUP		SAXENA, AKASH
1040 BROAD STREET		
2ND FLOOR		ART UNIT | PAPER NUMBER
SHREWSBURY, NJ 07702		2128

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

	Application No.	Applicant(s)
Office Action Summary	09/954,715	TSENG ET AL.
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 November 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-50 has/have been presented for examination based on amendment filed on 7th November 2006.

2. Claim(s) 7 and 9-10 is/are amended.

3. Claim(s) 9 remains objected to.

4. Claim(s) 1-50 remain rejected under 35 USC § 103.

5. The arguments submitted by the applicant have been fully considered. Claims 1-50 remain rejected and this action is made FINAL. The examiner's response is as follows.

Response to Applicant's Remarks & Examiner's Withdrawals

6. Examiner maintains the claim objection(s) to claim(s) 9 in view of the applicant's amendment. See below.

7. Examiner withdraws the claim rejection(s) under 35 USC § 112 to claim(s) 7-9 AND 10-18 in view of the applicant's amendment.

Response to Applicant's Remarks for 35 U.S.C. § 103

8. **Claims 1-6, 19-36, 38 & 44-46 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over U.S. Patent No. 5,663,900 issued to Narpat Bhandari et al

(BH '900 hereafter), in view of U.S. Patent No. 5771370 issued to Klein (Klein

hereafter).

Further, official notice was taken with U.S. Patent No. 6,052,524 Col.14 Lines 21-37

– Cited not used; U.S. Patent No. 5,546,562 – Abstract.

Regarding Claim 1

Examiner has stated in prior office action:

> *BH'900 further teaches that the second information comprises at least one internal state of the*
> *hardware model (BH'900: Col.3 Lines 21-29). Examiner takes official notice that in view of*
> *arguments presented in the last office action that such information would be vital to the any*
> *hardware-software co-simulation system.*
> BH'900 **does not explicitly teach** a shared memory for holding first information of software
> model and second information of the hardware model, and the software model is capable of
> directly accessing the second information of the hardware model.

The limitations being argued are:

> "shared memory for holding a first information of a software model and a second information of
> the hardware model, where the second information comprises at least one internal state of the
> hardware model and the software model is capable of directly accessing the second information
> of the hardware model."

Applicant has argued that evidentiary support teachings of U.S. Patent No.

6,052,524 and 5,546,562 do not indicate the information comprising at least one

internal state of the hardware model is "vital" to a co-simulation.

While the comments made by applicant are acknowledged, the references referred

to were to show the well-known state of the art. It is well known in the art that co-

simulation of hardware and software share information, otherwise it would not be

called co-simulation. Further the claim recites that the software model be "capable"

of accessing the second information, which is clearly taught by the prior art of U.S. Patent No. 6,052,524 and 5,546,562.

While the information sharing between the hardware and software model may be "vital" to instant invention, the claim as presented do not recite that, instead seem to make such sharing optional by the use of "capable". For this reason it is unclear if this even presents a limitation.

Further applicant has argued that Klein does not teach simulating the hardware portion of the design in hardware using an emulator or other type of reconfigurable hardware.

Examiner acknowledges applicant's comment however the claim does not recite simulating the hardware model in the emulator. Secondly, Klein is used in combination with BH'900 that teaches this limitation.

Further, applicant has argued that Klein teaches "single coherent view of memory" is not physical shared memory.

Examiner is first unclear how "single coherent view of memory" is patentably different than "physical shared memory" as long as the intended function of that hardware and software model see and share same information. Secondly, arguendo, even if they are different, the claim recites a "shared memory" and does not specifically disclosed a "physical shared memory". Further, the claim discloses a computing system and it is well known in the art the memory present in the computing system is shared by various application and peripherals (reconfigurable hardware attached via internal bus) attached to the computing system.

Further applicant has argued that the memory disclosed is not the memory of the

co-simulation system but memory portion of the design being co-simulated.

Applicant's comments are noted, however the claim does not make any such

distinction. Further, Fig.1 states, "Coherent view of the memory of hardware-

software simulation being co simulated", in contrast to the arguments being made.

Teaching of Klein is relevant to BH'900 as it teaches co-simulation having a

coherent memory to solve the at speed simulation problem between the hardware

and software models.

Regarding Claims 2-50

No new arguments were presented other than the combination of BH'900 and Klein

in view of common knowledge in the art is impermissible.

Examiner respectfully disagrees and maintains the rejectioN.

Applicant's argument regarding establishing a prima facie case of obviousness

are considered and are found to be unpersuasive.

Claim Objections

9. Claim 9 is objected to as it is unclear what is 1st trigger input is connected to, as the

claim 9, dependent on claim 8, only discloses, "…trigger signal is applied to the

second and third trigger inputs…". Further, claim 9 leaves the picture incomplete as

to what is connected to the "third logic input" of "a third logic". The amended claim

still does not clarify the connection between the components.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the

various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the

obligation under 37 CFR 1.56 to point out the inventor and invention dates of each

claim that was not commonly owned at the time a later invention was made in order

for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35

U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-6, 19-36, 38 & 44-46 are rejected under 35 U.S.C. 103(a) as being

unpatentable over U.S. Patent No. 5,663,900 issued to Narpat Bhandari et al

(BH '900 hereafter), in view of U.S. Patent No. 5771370 issued to Klein (Klein

hereafter).

Regarding Claim 1

BH '900 teaches an electronic design and automation (EDA) system for verification

and modeling a user design including a central processing unit (Sun Microsystems

Sparc workstation) (BH '900: Col.2, Lines 28-35; Col.1, Lines 14-18). Further, BH

'900 teaches an internal bus (SBus) system connected to the computing system (BH

'900: Col.2 Lines 46-50). Further, BH '900 teaches a reconfigurable hardware logic

(BH '900: Col.2 Lines 64-67; Col.3 Lines 1-2) coupled to the internal bus system (BH

'900: Col.3 Lines 14-17, 21-24; Figure 2A-2B, Elements 16,38,44 & 46) for

generating a hardware model which includes at least a portion of user design

modeled in hardware (BH '900: Col.3 Lines 56-67; Col.4 Lines 1-2). Further, BH

'900 teaches a controller/interface circuit (BH '900: Figure 2B, Element 40), which on

a card directly attached on the motherboard (BH '900: Figure 2B, Element 38, 36)

between the external systems (BH '900: Figure 2B, Element 44-46) and computing

system. The controller mentioned above, controls the flow of control data,

synchronization data, initialization of logic states or simulation model data to the

external systems likes field programmable gate array (FPGA) (BH '900: Col.5 Lines

7-15). Further, BH '900 teaches generating software models (BH '900: Col.1 Lines

25-28, Col.3 Lines 64-66) and hardware models (BH '900": Col.2 Lines 51-67; Col.3

Lines 1-2) and storing the models (BH '900: Col.3 Lines 2-5, 36-43).

BH'900 further teaches that the second information comprises at least one internal

state of the hardware model (BH'900: Col.3 Lines 21-29). Examiner takes official

notice that in view of arguments presented in the last office action that such

information would be vital to the any hardware-software co-simulation system[1].

BH'900 does not explicitly teach a shared memory for holding first information

of software model and second information of the hardware model, and the software

model is capable of directly accessing the second information of the hardware

model.

However, **BH'900 explicitly teaches** that communication between the software

model (prototype definition 32) and hardware model (on FPGA external system 44),

and signal processing there-between. BH'900: Col.3 Lines 21-29 states:

> Interface software and hardware is provided between the simulated prototype definition 32 and
> external systems 44, 46 to provide distributed or multiple access paths for cooperative processing
> and signal processing therebetween. In this manner, specified signal paths or interconnection
> lines are provided, as specified by a design engineer, from CAE tool 14 to particular sockets pins
> or electrical contacts or nodes in particular external systems 44, 46 from particular simulator 16.

To emphasize that the limitation relating to shared resource (memory

specifically), and direct access of the software model to the hardware model,

although obvious in BH'900, teachings of **Klein** are presented below.

Klein teaches shared (coherent) memory (Klein: Fig.1 Element 22) for holding

first information of software model (Klein: Fig.1 Element 34) and second information

---

[1] See evidentiary support in US Pat. 6,052,524 Col.14 Lines 21-37 – Cited not used; U.S. Patent No.
5,546,562 – Abstract - Cited not used.

of the hardware model (Klein: Fig.1 Element 38), and the software model is capable

of directly accessing the second information of the hardware model (Klein: Col.9

Fig.6 & related description; Col.11 Lines 48-49; Col.11 Line 63-Col.12 Line 9).

Here the first information is embodied as information present in the ISS 20,

second information is embodied in the form of hardware model processor instance

(Klein: Col.8 Lines 55-62).

Klein teaches the software model direct having direct access to the second

information bypassing the hardware model (simulation) using the co-simulation

optimization manager 27 (Klein: Col.11 Lines 48-49, Col.11 Line 63-Col.12 Line 9;

Fig.10).This kind of memory access is by software model (ISS 20) is understood to

be optimized access. Hardware accesses to the coherent memory are unoptimized

accesses. (See Col.4 Lines 15-36).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply teachings of **Klein** to **BH '900** to have a

coherent memory to solve the at speed simulation problem between the hardware

and software models (Klein: Col.2 Lines 18-30, 47-53; BH'900: Col.1 Line 54-Col.2

Line 13). The motivation to combine would be that Klein see BH'900 model as one

disclosed in Klein Col.2 Lines 18-20, as lacking speed, his invention enhances the

performance of BH'900 hardware-software model by providing the shared memory

concept with the co-simulation optimization manager 27.

Regarding Claim 2

BH '900 teaches first information of the software model including functional

information of the user design (BH '900: Col.1 Lines 25-35).

Regarding Claim 3

BH '900 teaches second information of the hardware model including functional

information of the user design (BH '900: Col.2 Lines 56-63).

Regarding Claim 4

BH '900 teaches hardware model includes the state information (BH '90: Col3. Lines

21-29, 51-55), which includes hardware node values and register-values

(Specification: Pg.60 Line 26).

Regarding Claim 5

BH '900 teaches SBus configuration and the controller connected directly to the

motherboard implementing the SBus (BH '900: Figure 2B Element 36-38; Col.2

Lines 46-50). DMA access is inherent to the SBus configuration (IEEE Std 1496-

1993)[2].

Regarding Claim 6

BH '900 teaches hardware model includes the state information (BH '900: Col3.

Lines 21-29, 51-55), which includes hardware node values and register-values

(Specification: Pg.60 Line 26).

---

[2] IEEE Standard for Boot Firmware: Bus Supplement for IEEE 1496 (SBus). – 18th November 1994

Regarding Claim 19

Method claim 19 discloses the similar limitations as claim 1 and is rejected for the

same reasons as claim 1. Further, **BH '900** teaches simulation method where the

software model imitates functional or logical output signals (*first* information) in

response to the stimulus applied (BH '900: Col.1 Lines 29-35).

Regarding Claim 20

Method claim 20 discloses the similar limitations as claim 5 and is rejected for the

same reasons as claim 5. *BH'900 further teaches that the third information asat*

least one internal state of the hardware model (BH'900: Col.3 Lines 21-29). Further,

please see argument presented in the last office action that such information would

be vital to the any hardware-software co-simulation system – see claim 1 evidentiary

support.

Regarding Claim 21

BH '900 teaches controlling the software and hardware model with a software kernel

(BH '900: Col.2 Lines 7-13; Col.6 Lines 1-7).

Regarding Claim 22

BH '900 teaches software kernel includes model input and output, which is parsed

and provided to the simulator through the PLI, thus allowing the simulation system to

determine the presence of input data. **BH '900** teaches a digital simulator using

Verilog; hence the *evaluation* of clock components[3] as part of the software program

(test bench) is inherent to the method of simulation. Further, **BH '900** teaches

propagating the input data to the hardware model (BH '900: Fig. 3; Col.6 Lines 34-62). Further, Examiner takes official notice that the step of detecting active clock edge of the clock in the software model is well known in the art[4]. Further, **BH '900** teaches evaluating the input data with the hardware model in response to the active clock edge detection (BH '900: Col.4 Lines 3-9, Col.5 Lines 7-15).

Regarding Claim 23

BH '900 teaches simulating the behavior of the software model for some time and then simulating the behavior of the circuit with hardware model for another time (BH '900: Col.3 Lines 61-67; Col.4 Lines 1-2, 18-24).

Regarding Claim 24

Method claim 24 discloses the similar limitations as claim 1 and is rejected for the same reasons as claim 1. Further, **BH '900** teaches simulating a behavior of the circuit with the software model by providing input data to software model (BH '900: Col.6 Lines 20-33). Further, **BH '900** teaches selectively switching to hardware model through software control and providing input data (BH '900: Col.5 Lines 10-15; 21-26). Further, **BH '900** teaches evaluating the input data in the hardware model based on the trigger event in the software model (BH '900: Col.5 Lines 7-10).

Regarding Claim 25

BH '900 teaches hardware model includes the state information (BH '90: Col3. Lines 21-29, 51-55), and it is stored in the shared memory (BH '900: Col.3 Lines 36-43).

---

[3] IEEE Std 1364-1995 IEEE standard hardware description language based on the Verilog(R) hardware description language. Cover Page & Pg. 101 with comments.
[4] IEEE Std 1364-1995: Cover Page & Pg. 370-371.

Regarding Claim 26

BH '900 teaches simulating the software model by using the state information (BH '900: Col.1 Lines 29-35) from hardware model in the shared memory (BH '900: Col.3 Lines 2-5, 36-43). Amendment to the claim does not change the response as the behavior of the circuit is the characteristic that being simulated by BH '900.

Regarding Claim 27

BH '900 teaches generating the hardware model further comprises of determining component type in hardware language and generating model based on the components (BH '900: Col.2 Lines 55-63; Col.3 Lines 51-55).

Regarding Claim 28

BH '900 teaches that portion of the user design can be simulated (in software) and portion of the user design can be emulated (in hardware) (BH '900:Col.3 Lines 61-64). Further, **BH '900** teaches selectively switching between hardware and software models (BH '900:Col.4 Lines 3-6). Further, **BH '900** teaches simulating the behavior of the circuit by providing input data to software model through the programmable logic interface (PLI) (BH '900: Figure 2A Elements 28, 30, 16).

Regarding Claim 29

BH '900 teaches software kernel includes model input and output, which is parsed and provided to the simulator through the PLI, thus allowing the simulation system to determine the presence of input data. **BH '900** teaches a digital simulator using Verilog; hence the evaluation of clock components (See Footnote 2 reference) as part of the software program (test bench) is inherent to the method of simulation.

Further, **BH '900** teaches propagating the input data to the hardware model (BH

'900: Fig. 3; Col.6 Lines 34-62).

Regarding Claim 30

Claim 30 discloses the similar limitations as claim 1 and is rejected for the same

reasons as claim 1. Claim 1 discloses steps of generating the software and

hardware models, allocating shared memory. Further, **BH '900** teaches propagating

data to the hardware model until data stabilizes as calculating the propagation delay

as part of the initialization setup (BH '900: Col.5 Lines 27-30). Further, **BH '900**

teaches detecting the clock edge being implicit to the Verilog model/test bench (See

IEEE Std 1364-1995). Further, **BH '900** teaches evaluating data with the hardware

model in response to the clock edge detection in software model and in

synchronization with a hardware-generated clock by external system/FPGA (BH

'900: Col. Lines 64-67).

Regarding Claim 31

Claim 31 discloses the similar limitations as claim 6 and is rejected for the same

reasons as claim 6.

Regarding Claim 32

BH '900 teaches simulating the software model by using the state information (BH

'900: Col.1 Lines 29-35) from hardware model in the shared memory (BH '900: Col.3

Lines 2-5, 36-43).

Regarding Claim 33

BH '900 teaches a simulation system operating in a host system for simulating the

behavior of a circuit (BH '900: Figure 2A-2B) containing CPU (BH '900: Col.2 Lines

51-55), shared memory (BH '900: Col.3 Lines 2-5, 36-43) and local bus coupling the

CPU to memory (BH '900: Col.2 Lines 46-50). BH '900 teaches a circuit having

structure and function in a hardware language capable of describing the component

types and connection (BH '900: Col.2 Lines 56-63; Col.3 Lines 48-55).

Further, BH '900 teaches software model coupled to the local bus (BH '900: Figure

2A Elements 16-34-36), software control logic (BH '900: Figure 2A Element 30)

coupled to the software model & hardware logic element (BH '900: Figure 2A-2B

Elements 38, 40, 42-46) for controlling the operation of software model and

hardware logic element. Further, BH '900 teaches hardware logic element coupled

to local bus (BH '900: Figure 2B Elements 36-38) and hardware model including at

least a portion of the circuit (BH '900: Col.3 Lines 61-67; Col.4 Lines 1-2) configured

automatically based on component type (BH '900: Col.3 Lines 48-54).

Further, BH '900 teaches SBus configuration and the controller connected directly to

the motherboard implementing the SBus (BH '900: Figure 2B Element 36-38; Col.2

Lines 46-50). DMA engine based access is inherent to the SBus configuration.

__BH'900 further teaches that the second information comprises at least one internal__

__state of the hardware model (BH'900: Col.3 Lines 21-29). Further, please see__

__argument presented in the last office action that such information would be vital to__

__the any hardware-software co-simulation system.__

BH'900 further teaches *the software model is capable of directly accessing the second information of the hardware model (Klein: Col.9 Fig.6 & related description; Col.11 Lines 48-49; Col.11 Line 63-Col.12 Line 9).*

Regarding Claim 34 & 35

Claims 34 & 35 discloses the similar limitations as claim 21 & 22 and are rejected for the same reasons as claims 21 & 22.

Regarding Claim 36

BH '900 teaches hardware logic element comprises a field programmable device (BH '900: Col.3 Lines 1-2).

Regarding Claim 38

Claim 38 discloses the similar limitations as claim 1 and is rejected for the same reasons as claim 1. Further, BH '900 teaches control logic coupled to internal bus system for delivering the data among reconfigurable hardware logic and computing system (BH '900: Fig. 3; Col.6 Lines 34-62).

Regarding Claim 44

Claim 44 discloses the similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 45

BH '900 teaches synchronizing the data evaluation in the software model and hardware model with software configured/generated clock (BH '900: Col.5 Lines 64-67).

Regarding Claim 46

BH '900 teaches simulating selected debug test points in the software as software

program (kernel) which can control the simulation flow by starting, stopping, single-

stepping, interrupting, or polling the simulation (BH '900: Col.6 Lines 5-7).

Further, BH '900 teaches accelerating selected portions in hardware (BH '900: Col.3

Lines 61-67, Col.4 Lines 1-2). Further, BH '900 teaches controlling the delivery of

data between the hardware and software model through the external I/O so that

software model has access to all delivered data (BH '900: Col.4 Lines 39-46).

11. Claim 7 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

U.S. Patent No. 5,663,900 issued to Narpat Bhandari et al (BH '900 hereafter),

in view of U.S. Patent No. 5771370 issued to Klein (Klein hereafter), further in

view of IEEE article "Q-Modules: Internally clocked Delay-Insensitive Modules"

by Fred U. Rosenberger et al (RO '1988 hereafter).

Regarding Claim 7

Teachings of BH '900 are disclosed on claim 1 rejections above.

BH '900 does not teach timing logic associated with each flip flop so the desired

result is obtained regardless of the order of arrival of a input and a clock signal to the

flip flop.

RO '1988 teaches their Q-modules are insensitive to delay and that the inputs

must be able to accept inputs that change at any time with respect to the clock and

must operate correctly in the presence of metastability (RO '1988: Pg.1006 Section

II; Pg 1009 Section III D).

Motivation to combine Klein with BH'900 is provided in claim 1 rejection above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply teachings of RO '1988 to BH '900 to make

logic elements that are delay insensitive. The motivation to combine would have

been that BH '900 is designing a hardware emulated and software simulated co

simulation system, where parasitic effects of propagation delays between the

hardware and software boundaries are of concern (BH '900: Col.5 Lines 27-30) and

RO '1988 solves this problem by teaching that Q-modules which can be at the

interface of simulation environment and FPGA hardware boundary where such

metastable transitions are most possible (RO '1988: Pg. 1005 Last paragraph).

Further, motivation would have been that RO '1988 discloses that Q-modules are

used in the personalizing the PLAs (Abstract).

Regarding Claim 10

Claim 10 discloses the similar limitations as claim 7 and is rejected for the same

reasons as claim 7.

12. Claims 8-9 & 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable

over U.S. Patent No. 5,663,900 issued to Narpat Bhandari et al (BH '900

hereafter), in view of U.S. Patent No. 5771370 issued to Klein (Klein hereafter),

further in view of IEEE article "Q-Modules: Internally clocked Delay-Insensitive

Modules" by Fred U. Rosenberger et al (RO '1988 hereafter), further in view of

IEEE article "High Speed External Asynchronous/Internally clocked Systems"

by W.S. VanScheik et al (VA '1997 hereafter).

Regarding Claim 8 & 9

Teachings of **BH '900** & **RO '1988** are disclosed on claim 1 rejections above.

BH '900 does not teach timing logic having a first logic, second logic, third logic

and edge detector.

RO '1988 also does not teach the exactly the disclosed limitations for the first

logic, second logic, third logic and edge detector. However the solve the same

problem as disclosed by the limitations.

VA '1997 teaches a first logic (VA '1997: Fig.5 Input Registers & Next State

Logic) having first input (VA '1997: Fig 5 INPUTS), a second input (VA '1997: Fig.5

Second feedback input to Next State Logic), a control input (VA '1997: Fig.5 Clock

signal to the Input registers) and an output (VA '1997: Fig.5 output of Next State

Logic). Further, **VA '1997** teaches a second logic (VA '1997: Fig.5 Memory

Registers) with first trigger input (VA '1997: Fig.5 Clock) and first logic output

coupled to the second input of the first logic (VA '1997: Fig.5 Memory register output

to the next state logic) where second logic updated the first logic. Further, **VA '1997**

teaches a third logic storing the new value (VA '1997: Fig.5: Output Logic). Further,

VA '1997 teaches a edge detector having a third trigger and clock input and output

is coupled to the control input (VA '1997: Fig.5: Majority Gate & Clock Driver).

The limitation "first trigger input" is taught by the prior art (VA '1997: Fig.5 Clock -

first trigger input). *The limitation "new value of first data" provided in claim 9 is still*

taught by the prior art in as a third logic storing the new value (VA '1997: Fig.5:

Output Logic). Further, examiner takes official notice that edge detectors are well

known in the art[5].

>   *Motivation to combine **Klein** with **BH'900** is provided in claim 1 rejection above.*

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply teachings of **RO '1988 to BH '900** to make

logic elements that are delay insensitive. The motivation to combine would have

been that **BH '900** is designing a hardware emulated and software simulated co

simulation system, where parasitic effects of propagation delays between the

hardware and software boundaries are of concern (**BH '900**: Col.5 Lines 27-30) and

RO '1988 solves this problem by teaching that Q-modules which can be at the

interface of simulation environment and FPGA hardware boundary where such

metastable transitions are most possible (RO '1988: Pg. 1005 Last paragraph).

Further, It would have been obvious to one (e.g. a designer) of ordinary skill in

the art at the time the invention was made to apply teachings of **VA '1997 to BH**

'900 to make logic elements that are delay insensitive. The motivation would have

---

[5] U.S. Patent No. 5808486, Figure 1

been that **VA '1997** further refines the work of **RO '1988** (VA '1997: Pg824, Col.2

Lines 1-2) and handles the propagation delay issues across asynchronous

interfaces like in **BH '900** (VA '1997: Abstract: Lines 1-4) to avoid metastability.

Regarding Claim 11

VA '1997 teaches an timing circuit with input logic (VA '1997: Fig.5 Input Registers &

Next State Logic) for receiving the input value and trigger signal (VA '1997: Fig 5

INPUTS, Clock), a storage logic (VA '1997: Fig.5 Memory Registers), a transmission

logic (VA '1997: Fig.5: Output Logic) coupled to the input logic and storage logic for

selecting between the new and old values and outputting it. Further, **VA '1997**

teaches an edge detecting logic (VA '1997: Fig.5: Majority Gate & Clock Driver).

VA '1997 teaches a selection logic (VA '1997: Fig.5: Output Logic) coupled to the

input logic and storage logic for selecting between the new and old values and

outputting it.

Regarding Claims 12-18

The limitations of claims 12-18 recite "D-Flip Flop", multiplexers, AND gates, OR

gates etc. The examiner has interpreted these elements to be functionally equivalent

to the circuit disclosed by VA '1997 (VA '1997: Fig.3, 5 & 6). *VA '1997 teaches a*

selection logic (VA '1997: Fig.5: Output Logic) coupled to the input logic and storage

logic for selecting between the new and old values and outputting it.

13. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S.

Patent No. 5,663,900 issued to Narpat Bhandari et al (BH '900 hereafter) in view

of U.S. Patent No. 5771370 issued to Klein (Klein hereafter), further in view of

U.S. Patent No. 5,661,662 issued to Michael R. Butts et al (BU '662 hereafter).

Regarding Claim 37

Teachings of **BH '900** are disclosed on claim 33 rejections above.

BH '900 does not teach plurality of field programmable devices coupled together

separable by at most two interconnection.

BU '662 teaches plurality of field programmable devices coupled together (BU

'662: Figure 3) separable by at most two interconnection (BU '662: Figure 7; Col.11

Lines 33-43).

Motivation to combine **Klein with BH'900** is provided in claim 1 rejection above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply teachings of **BU '662** to **BH '900** to make a

multi FPGA system coupled together. The motivation would have been, as **BU '662**

teaches, generally it takes more than one FPGA to implement the desired design

(BU '662: Col.3 Lines 3-31) for any practical system. Hence **BH '900** design would

also require more than one FPGA to implement the design and **BU '662** teaches

how to implement a multiple FPGA design while handling the interconnect issue

through the Realizer technology by Quickturn.

14. Claims 39-43 & 47-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,663,900 issued to Narpat Bhandari et al (BH '900 hereafter) in view of U.S. Patent No. 5771370 issued to Klein (Klein hereafter), further in view of IEEE article "A Heterogeneous Environment for Hardware/Software Cosimulation" by William D. Bishop et al (BI '1997 hereafter).

Regarding Claim 39

Claim Interpretation:

"Data-in pointer logic" and "Data-in latch logic" are together interpreted as hybrid decoder and cross-point router. "Data-in pointer logic" is generating the select signal based on the source of data present on the internal bus and "Data-in latch logic" routes the data based on the select signal to the selective internal nodes in the reconfigurable hardware.

Teachings of **BH '900** are disclosed on claim 38 rejections above.

BH '900 does not teach plurality of field programmable devices "Data-in pointer logic" and "Data-in latch logic" with the disclosed limitations.

BI '1997 teaches an interface platform (BI '1997: Pg.15 Section 2.3; 4.2) that performs the function of directing the data from the internal data bus to the various FPGA's based on the external interface or computing system (BI '1997: Fig.1, 3). For example: The external interface may be the development platform and the computing system may be the software simulation platform. Further, the limitations

"Data-in pointer logic" and "Data-in latch logic" disclosed are obvious by necessity in

the described interface.

Motivation to combine **Klein with BH'900** is provided in claim 1 rejection above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at

the time the invention was made to apply teachings of **BI '1997** to **BH '900** to design

an interface control logic. The motivation would have been that **BI '1997** is

addressing the same issues as **BH '900** to perform hardware/software co-simulation

using the Sun Sparc station and FPGA's (BI '1997: Figure1, 2). Further, **BH '900**

also discloses a pin arrangement for the interface circuit between the hardware and

software (BH '900: Fig.3).

Regarding Claim 40

BI '1997 teaches an external buffer for storing the external data from the external

interface so the data is mutually accessible by buffer and the computing system (BI

'1997: Pg.18 Col.2 6th paragraph; Section 4.2 1st paragraph).

Regarding Claim 41

Claim 40 recites the similar limitation as claim 39 but data is transferred in the

opposite direction. **BI '1997** teaches a bidirectional interface to monitor and seed the

simulation (BI '1997: Fig.2) as well as configures the FPGA's (BI '1997: Pg. 15 Col.1

Last paragraph).

Regarding Claim 42

BI '1997 teaches control and data signal being sent back between the software

simulation and the hardware emulation (BI '1997: Fig.2). Further, detection of

software clock and evaluation in well known in the art and obvious by necessity of

the current co-simulation design (See IEEE Std 1364-1995 reference cited before).

Regarding Claim 43

BI '1997 teaches selecting which components of the design as hardware and

software entities and describes the reasoning why one would select a component to

be simulated rather than being emulated (BI '1997: Section 3). It is obvious from the

discussion the reasons why some of the external I/O would be simulated rather

being emulated (i.e. emulation is performed for components where timing &

implementation details are necessary and simulation is performed where

functionality needs to be checked).

Regarding Claim 47

Claim 47 discloses the similar & subset of limitations as claim 39 and is rejected for

the same reasons as claim 39.

Regarding Claim 48

Claim 48 discloses the similar limitations as claim 40 and is rejected for the same

reasons as claim 40.

Regarding Claim 49

Claim 49 discloses the similar limitations as claim 39 and is rejected for the same

reasons as claim 39.

Regarding Claim 50

Claim 50 discloses the similar & subset of limitations as claim 43 and is rejected for

the same reasons as claim 43.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and

any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

date of the advisory action. In no event, however, will the statutory period for reply

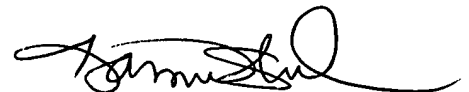expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Friday, January 19, 2007

Kamini S. Shah
Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation